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REMARKS

Claims 1, 3-18, 20-32 and 39 are currently pending in the above-identified application. Claims 1, 3-18, 20-32 and 39 have been rejected. Claims 1, 11, 18 and 25 have been amended. Applicant respectfully requests reconsideration in light of the foregoing amendments and following remarks.

Claims 1, 3-4, 9-12, 15-16, 18-19 and 22-24 stand rejected under 35 U.S.C. §102(b) as being anticipated by Chiang et al. Applicant respectfully traverses the rejection.

The claims of the present application are directed to a semiconductor structure that includes an etch stop layer which allows for positioning of vias extending down to a conductive plug without encountering the attendant disadvantages associated with zero or negative overlap of the vias relative to the plug. Overlap can lead to an air gap, which may trap air within the structure or device.

Claim 1, as amended, recites a semiconductor structure that includes "an insulator layer", "a conductive plug positioned within said insulator layer and formed of a single conductive material", "a doped region connected to said conductive plu", "an etch-stop layer located on said insulator layer and surrounding said plug", "a non-conductive layer having an etched via at least partially over said conductive plug", and "a conductive connector formed in said via in electrical contact with said plug and including a first conductive layer deposited in and in contact with said etched via and a second conductive layer deposited over and in contact with said first conductive layer, said first conductive layer including a portion in contact with said conductive plug". Claims 3-4 and 9-10 depend from claim 1.

Claim 11, as amended recites a semiconductor device that includes "at least one memory cell". The memory cell comprises "an active region in a substrate", "a conductive plug positioned within an insulator layer and provided over said active region, said conductive plug being electrically connected with said active region", "an etch-stop layer deposited on said insulator and around said conductive plug", "an intermediate non-conductive layer provided over said etch stop layer and having at least a first and a second etched via over said plug, wherein said second etched via is above and has a greater diameter than said first etched via", and "at least one conductive layer in said first and second vias in electrical connection with said plug". Claims 12 and 15-16 depend from claim 11.

Claim 18, as amended, recites a semiconductor device that includes "a conductive element formed of a single conductive material", "an etch-resistant layer surrounding an upper portion of said conductive element", "a non-conductive layer over said etch resistant layer and having a via over said conductive element, said via extending down to a level of said conductive element and etch resistant layer", "a conductive material located in said via, wherein said conductive material in said via contacts said conductive element", and "a doped region connected to said conductive element". Claims 19 and 22-24 depend from claim 18.

Chiang et al. discloses to a semiconductor device having interconnections. The device of Chiang et al. includes a conductive plug, formed of a layer of titanium nitride 40 surrounding a tungsten layer 41, within a BPSG layer 22, an etch-stop layer 23, a barrier layer 60 and a metal layer 61. The barrier layer 60 and metal layer 61 fit within an

interconnect channel 51, which is shown as an opening having a single diameter. Additional interconnect channels are shown, such as opening 330 (FIG. 16), opening 353 (FIG. 20), and interconnect channel 351 (FIGS. 21, 22), all of which are openings having a single diameter.

Chiang et al. fails to teach or suggest "a conductive plug positioned within said insulator layer and formed of a single conductive material" and "a doped region connected to said conductive plug" as recited in claims 1, 3-4 and 9-10, or "a conductive element formed of a single conductive material" as recited in claims 18-19 and 22-24. Chiang et al. also fails to teach or suggest "at least a first and a second etched via over said plug, wherein said second etched via is above and has a greater diameter than said first etched via" and "at least one conductive layer in said first and second vias" as recited in claims 11-12 and 15-16. A conductive plug formed of a single conductive material simplifies processing by eliminating one or more fabrication steps. Having at least a pair of vias of different diameters allows a greater surface area for the conductive material located in the first and second vias than is possible in a single via, as shown in Chiang et al. Since Chiang et al. fails to teach or suggest all the elements of claims 1, 3-4, 9-10, 18-19 and 22-24, applicant respectfully submits that these claims cannot be anticipated by this reference.

Claims 5-6, 17, 25-27, 30-32 and 39 stand rejected under 35 U.S.C. §103 as being unpatentable over Chiang et al. in view of Wang et al. Applicant respectfully traverses the rejection.

Claims 5-6 are dependent on claim 1 and claim 17 is dependent on claim 11 discussed above. Claims 25-27, 30-32 and 39 recite a processor-based system that includes

"a processing unit" and "a semiconductor circuit coupled to said processing unit". The semiconductor circuit includes "a conductive plug positioned within an insulator and provided on a connection region", "an etch-stop layer deposited on said insulator, said etch-stop layer being at the same level as a top portion of said conductive plug", "an intermediate non-conductive layer provided over said etch-stop layer and having at least a first and a second etched via over said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via", and "a conductive connector electrically coupled to said connection region, said conductive connector comprising a first conductive layer deposited in and in contact with said first and a second etched vias, said first conductive layer including a portion in contact with said conductive plug".

Wang et al. refers to a method of using a thin resist mask for a dual damascene stop layer etch. Claims 5-6 depend from claim 1, and the arguments provide above with reference to the rejection of claim 1 are equally applicable here. Specifically, like Chiang et al. discussed above, Wang et al. fails to teach or suggest "a conductive plug positioned within said insulator layer and formed of a single conductive material" and "a doped region connected to said conductive plug" as recited in claims 5-6. Claim 17 depends from claim 11, and the arguments provided above with reference to the rejection of claim 11 are equally applicable here. Specifically, Wang et al. fails to teach or suggest "an intermediate non-conductive layer provided over said etch-stop layer and having at least a first and a second etched via ... wherein said second etched via is above and has a greater diameter than said first etched via" and "at least one conductive layer in said first and second vias in electrical connection with said plug" as recited in claim 17. Wang et al. further fails to

teach or suggest "an intermediate non-conductive layer provided over said etch-stop layer and having at least a first and a second etched via ... wherein said second etched via is above and has a greater diameter than said first etched via" and "a conductive connector ... comprising a first conductive layer deposited in and in contact with said first and second etched vias" as recited in claims 25-27, 30-32 and 39.

Since the cited references fail to disclose or suggest all the recited features, the subject matter of claims 5-6, 17, 25-27, 30-32 and 39 would not have been obvious in light of the combination of Chiang et al. with Wang et al.

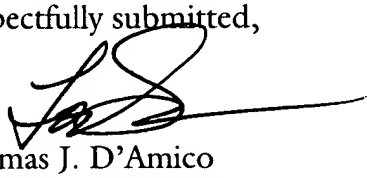
Claims 7-8, 13-14, 20-21 and 28-29 stand rejected under 35 U.S.C. §103 as being unpatentable over Chiang et al. in view of Hong et al. Applicant respectfully traverses the rejection.

Claims 7-8 depend from claim 1, claims 13-14 depend from claim 11, claims 20-21 depend from claim 18, and claims 28-29 depend from claim 25. The arguments provided in the above rejections are equally applicable here. Hong et al., like the other cited references, fails to teach or suggest at least two vias, with one via being above and having a greater diameter than the other via, and a conductive connector within both of the vias. Further, Hong et al. fails to teach or suggest a conductive plug formed of a single conductive material and a doped region connected to the conductive plug. Since the cited references fail to disclose the recited invention, the subject matter of claims 7-8, 13-14, 20-21 and 28-29 would not have been obvious in light of the combination of Chiang et al. with Hong et al.

For at least the reasons provided above, applicant believes that each of the presently pending claims is in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: October 24, 2001

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 1, 11, 18 and 25 have been rewritten.

1. (Twice Amended) A semiconductor structure comprising:

an insulator layer;

a conductive plug positioned within said insulator layer and formed of a single conductive material;

a doped region connected to said conductive plug;

an etch-stop layer located on said insulator layer and surrounding said plug;

a non-conductive layer having an etched via at least partially over said conductive plug; and

a conductive connector formed in said via in electrical contact with said plug and including a first conductive layer deposited in and in contact with said etched via and a second conductive layer deposited over and in contact with said first conductive layer, said first conductive layer including a portion in contact with said conductive plug.

11. (Amended) A semiconductor device comprising:

at least one memory cell comprising:

an active region in a substrate;

a conductive plug positioned within an insulator layer and provided [on] over said active region, said conductive plug being [in contact]

electrically connected with said active region;

an etch-stop layer deposited on said insulator and around said conductive plug;

an intermediate non-conductive layer provided over said etch stop layer and having [an] at least a first and a second etched via over said [plug] plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

at least one conductive layer in said [via] first and second vias in electrical connection with said plug.

18. (Twice Amended) A semiconductor device comprising:

a conductive element formed of a single conductive material;

an etch-resistant layer surrounding an upper portion of said conductive element;

a non-conductive layer over said etch resistant layer and having a via over said conductive element, said via extending down to a level of said conductive element and etch resistant layer;

a conductive material located in said via, wherein said conductive material in said via contacts said conductive element; and

a doped region connected to said conductive element.

25. (Amended) A processor-based system comprising:

a processing unit;

a semiconductor circuit coupled to said processing unit, said semiconductor circuit comprising:

[a substrate supporting a connection region;]

a conductive plug positioned within an insulator and provided on [said] a connection region;

an etch-stop layer deposited on said insulator, said etch-stop layer being at the same level as a top portion of said conductive plug;

an intermediate non-conductive layer provided over said etch-stop layer and having [an] at least a first and a second etched via over said conductive [plug] plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

a conductive connector electrically coupled to said connection region, said conductive connector comprising a first conductive layer deposited in and in contact with said first and second etched [via] vias, said first conductive layer including a portion in contact with said conductive plug.